ABSTRACT

A clock system for a data bus, e.g., a memory bus system, provides a write data (WCLK) clock signal in one direction on a bus and a data read (RCLK) clock signal in an opposite direction on the bus. A predetermined phase relationship between said WCLK and RCLK clock signals is set at a predetermined location on the data bus to ensure that all memory subsystems connected to the bus receive the WCLK and RCLK signals with appropriate timing to ensure proper operation of the memory subsystems.